59. (New) A computer processor for coupling to a memory system in a multiple-processor computer system, said processor comprising an instruction processor configured to process instructions according to an instruction-set architecture whose semantics enable interaction with the memory system according to a memory model in which a local memory subsystem is accessible to the computer processor and a common memory subsystem accessible to all the processor of the multiple-processor system, said architecture including a plurality of types of memory access instructions, the types of memory access instructions including:

a local store instruction specifying a value and an address in the memory system wherein the semantics of said instruction require that prior to completion of the instruction the value is stored at said address in the local memory subsystem or the common memory subsystem without necessarily requiring that the value is stored in the common memory subsystem;

an instruction specifying an address in the memory wherein the semantics of said instruction require that a value previously stored at the specified address in the local memory subsystem was previously stored at that address in the common memory subsystem or will be stored at said address in the common memory subsystem prior to completion of the instruction;

an instruction specifying an address in the memory wherein the semantics of said instruction require that prior to completion of the instruction the local memory subsystem holds a value at said address that was previously stored at that address in the common memory subsystem;

a local load instruction specifying an address in the memory system wherein the semantics of said instruction require a value stored at said address in the local memory subsystem or in the common memory subsystem to be retrieved by the processor.

REMARKS

Claims 2-26 were cancelled by preliminary amendment. Claim 1 stands rejected under double patenting over the claim 1 of US Pat. 6,636,950, as well as under 35 USC 102(b) over Liencres (US Pat. 5,765,196). Without conceding to the positions taken in the office action, the applicant has cancelled remaining claim 1 and added new claims 27 through 59, including new independent claims 27, 49, 52, and 59, to more clearly point out what is being claimed. The techniques described in Liencres do not anticipate or make obvious these claims. For example, with regard to claim 27, Liencres does not disclose or suggest "a first class of instructions whose semantics enable access a local memory for the processor without requiring coordination of data updates in a memory address space between the local memory and the shared memory system". As another example, with regard to claim 49, Liencres does not disclose or suggest "the instruction set including: instructions enabling uncoordinated memory access to the local memory system of a processor; and instructions enabling coordinated memory access by multiple processors."

Please apply $175.00 for excess claim fees and any other charges or credits to deposit account 06-1050 referencing docket number 01997-242002.

Respectfully submitted,

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